In the Specification:

Please amend the specification as follows:

Please replace the first paragraph on Page 3, starting at Line 1, with the following rewritten paragraph:

While the prior art patents describe the system, circuitry, functioning, and timing of pixel circuits and APS. None of the patents include any aspects of testing apparatus and methods for testing functionality, evaluating performance or determining capacitance of an APS[[..]].

Please replace the last paragraph on Page 3, starting at Line 15 and extending to Page 4, with the following rewritten paragraph:

The gate of the transistor M2 is connected to a reset terminal to receive the reset signal V_{rst}. The sensor readout node FD, that is the anode of the photo-diode D_F, is first reset to a high voltage level (V_{DD}) by changing the reset signal V_{rst} from a low voltage level (0) to a high voltage level (V_{DD}) to charge the capacitance C_{FD}. At the completion of charging the capacitance C_{FD}, the reset signal V_{rst} is changed from the high voltage level (V_{DD}) to the low voltage level. Since light is shown on the photo-diode D_F, photo-generated electrons are collected at node FD and the voltage at the node FD decreases in the process. At the end of the exposure duration the voltage at node FD is measured, thus completing one photo-sensing cycle. The photo-sensing cycle is completed by

deactivating the transistor M3 by changing the row select signal from the high voltage level (V_{DD}) to the low voltage level (0).

Please replace the first paragraph on Page 6, starting at Line 10, with the following rewritten paragraph:

The voltage source VS1 driving the supply line $V_{DD}1$ is set to a voltage level of the power supply voltage ~~source V_{DD}~~ source V_{DD}. A second voltage source connected to the $V_{DD}2$ line is also set to the same value, the power supply voltage ~~source V_{DD}~~ source V_{DD}. Bright light is shown on the pixel so that it is saturated. The reset signal V_{rst} is pulsed periodically and the resulting average current from the voltage source is measured. The equation relating the measured average current I and the capacitance C_{FD} on the node FD of the photo-diode D_F is calculated by the formula:

Please replace the first paragraph on Page 29, starting at Line 4, with the following rewritten paragraph:

The operational mode for the testable APS cell of this invention is activated by closing switch S1 to connect the voltage level V1 to the read distribution line RD. During the normal operation, the voltage level V1 is set to the level of the power supply voltage ~~source V_{DD}~~ source V_{DD}. The testable APS pixel cell is reset by turning on the transistor M2 bringing the reset line V_{rst} to a high level. The capacitance C_{FD} is charged to the voltage level V1 which turns on th transistor M1. The row select signal V_{row} is then activated and the reference

level of the node FD is sampled by the signal conditioning and readout circuit Sig C/R as described above. The reset signal line V_{rst} disables the transistor M2. The light exposes the photodiode D_F and as described above, electrons are collected at the node FD. After an integration time, the signal conditioning and readout circuit Sig C/R senses the collected charge of the node FD, conditions the signals and provides the readout as also described above.

Please replace the first paragraph on Page 36, starting at Line 5, with the following rewritten paragraph:

The reference sample and hold signal SHR changes from the low voltage level (0V) to the high voltage level (V_{DD}) at the time t_7 to activate the signal conditioning and readout circuit Sig C/R to sample and retain the reference voltage level. The reference sample and hold signal SHR is changed from the high voltage level (V_{DD}) to the low voltage level (0V) at the time t_8. The sensed signal output V_{sig_out} and the reference signal output V_{rst_out} are differentially compared to determine the voltage that is present at each node FD of each pixel. Since the voltage at each node FD of each pixel varies ~~incrementally~~ incrementally from the voltage level V2 to the voltage level V1, the output voltage of the signal conditioning and readout circuit Sig C/R will vary ~~incrementally~~ incrementally, dependent on the position of the connection of each to the resistor string R_1, R_2,..., R_{n-1}, R_n. Since the values of the voltage level V1 and V2 are known, the linearity and functioning of the pixel and the int rmediate circuitry can be determined. Fig. 8 shows the results of testing a row of pixels as described

above. As each pixel in the row is evaluated, the voltage level is recorded according to its position on th row. As is shown, the voltage level varies incrementally between zero volts and the difference between the voltage levels **V1** and **V2** depending on its position in the row and its connection location to the resistor string R_1, R_2,..., R_{n-1}, R_n.